Lehrstuhl für Technische Elektronik der Technischen Universität München

Control of Harmful Effects during the Program Operation in NAND Flash Memories

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Vollständiger Abdruck der von der Fakultät für Elektrotechnik und Informationstechnik der Technischen Universität München zur Erlangung des akademischen Grades eines

Doktor-Ingenieurs

genehmigten Dissertation.

Vorsitzender: Univ.-Prof. Dr. rer. nat. G. Wachutka

Prüfer der Dissertation:

- 1. Univ.-Prof. Dr. rer. nat. D. Schmitt-Landsiedel
- 2. Univ.-Prof. Dr.-Ing. Chr. Jungemann Rheinisch-Westfälische Technische Hochschule Aachen

Die Dissertation wurde am 13.04.2011 bei der Technischen Universität München eingereicht und durch die Fakultät für Elektrotechnik und Informationstechnik am 28.07.2011 angenommen.

Selected Topics of Electronics and Micromechatronics Ausgewählte Probleme der Elektronik und Mikromechatronik

Volume 42

Christoph Friederich

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Shaker Verlag Aachen 2011

Bibliographic information published by the Deutsche Nationalbibliothek

The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available in the Internet at http://dnb.d-nb.de.

Zugl.: München, Techn. Univ., Diss., 2011

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Printed in Germany.

ISBN 978-3-8440-0586-8 ISSN 1618-7539

Shaker Verlag GmbH • P.O. BOX 101818 • D-52018 Aachen Phone: 0049/2407/9596-0 • Telefax: 0049/2407/9596-9 Internet: www.shaker.de • e-mail: info@shaker.de

Meiner Familie

"I may not have gone where I intended to go, but I think I have ended up where I needed to be." Douglas Adams

Abstract

The dissertation on hand presents research on NAND flash memories, which are the most recent of today's dominant memory technologies. Its market growth fueled the cut of its product cycles to about one year and also led to increasing diversity of NAND flash products. Both make the evolutionary research and development strategy difficult to handle. Therefore, it is in urgent need to evaluate the interactions of design and technology as well as the impact of intrinsic variations and of growing harmful effects on the cells' stored information as soon as possible in the development phase of the flash memory system. However, this requires models for cell - system interaction, which are able to link the physical and electrical properties of the memory transistors with the behavior of the memory system to support the systematic decision on trade offs.

For this purpose, this work discusses the cell physics of the non-volatile semiconductor memory cell as well as its write mechanisms. The direct interaction between the programming algorithm and physical cell parameters is investigated. The NAND memory array architecture and its implications on cells' read and program operations are presented. Harmful effects on the stored information are presented, categorized, analyzed, and for this purpose conceptually separated in disturb and noise effects. Algorithmic countermeasures for floating gate cross coupling, which was seen as major blocking point for future scaling, are proposed. It is shown by worst case analysis, that floating gate cross coupling can be efficiently controlled by algorithmic countermeasures.

Taking other harmful effects into account requires a more general and versatile analysis approach. Therefore a stochastic model for the program operation is derived and experimentally verified at 48 nm ground rule. The utility and flexibility of this model is demonstrated by discussing the control of cells' V_{th} by a weak programming strategy, and by the optimization of the transistor geometry for increased V_{th} control, respectively. This improved control may be used in future NAND flash memories to either improve the memory reliability or to increase the stored data density according to the requirements of the targeted application.

By including more and more of the previously discussed harmful effects into the model for cell-system interaction, it could mature to a complete NAND memory simulator. This dissertation demonstrates the feasibility of such an approach and establishes the theoretical foundations. ii

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Abbreviations and Symbols

Abbreviations

16LC	16 Level Cell
8LC	8 Level Cell
AA	Active Area
AGL	Array Ground Line
BL	Bit Line
BPD	Background Pattern Dependency
BSEL	Block SElector Lines
ВТВНН	Band To Band Hot Hole
CC	Cross Coupling
CD	Coupling Dielectric
CG	Control Gate
CHE	Channel Hot Electron
\mathbf{CTF}	Charge Trapping Flash
DRAM	Dynamic Random Access Memory
ECC	Error Correcting Code
EEPROM	Electrical Erasable Programmable ROM
ЕОТ	Equivalent Oxide Thickness
EPROM	Erasable Programmable ROM
ETOX	Erase Through OXide
F	minimal feature size

FETMOS	Floating-gate Electron Tunneling MOS
\mathbf{FG}	Floating Gate
FLOTOX	FLOating-gate Tunneling OXide
FN	Fowler Nordheim
GP	Gate Plugs
GSL	Ground Select Line
GWL	Global Word Lines
HDD	Hard Disk Drives
IC	Integrated Circuit
IPD	Inter Poly Dielectric
ISPP	Incremental Step Pulse Programming
ITRS	International Technology Roadmap for Semiconductors
IWD	Inter Word line Dielectric
LRD	Local Row Decoder
LSB	Least Significant Bit
MC	Monte-Carlo
MLC	Multi Level Cell
MNOS	Metal Nitride Oxide Seminconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NOP	Number Of Programs
NVM	Non-Volatile Memory
NVSM	Non-Volatile Semiconductor Memory
OTP	One Time Programmable
PAE	Program After Erase
PROM	Programmable-ROM
PV	Program Verify

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Abbreviations and Symbols

Program Weak
Random Access Memory
Read Only Memory
Random Telegraph noise
Self Aligned-Shallow Trench Isolation
Self Boosted Erase Inhibit
Self Boosted Negative Verify
Self Boosted Program Inhibit
Source Line
Source Line Noise
Silicon On Insulator
Silicon-Oxide-Nitride-Oxide-Silicon
Static RAM
Solid State Disk
String Select Line
Shallow Trench Isolation
Tunneling Dielectric
Word Line

Symbols

*	Convolution	
$A_{cc,i}$	Area facing the <i>i</i> th adjacent cell.	$\left[\mathrm{cm}^{2} ight]$
α	Gate coupling ratio of the capacitance of the coupling dielect overall floating gate capacitance.	ric to the
α_{cc}	Word line coupling ratio of the inter word line capacitance word line capacitance.	e and the
AR	Accuracy Range parameter of verify functions in the mode grammed V_{th} distributions.	el of pro- [V]
b	Number of bits stored in a single memory cell.	
C_{BL}	Overall bit line capacitance.	$[\mathbf{F}]$
C_{cell}	Simplified cell capacitance of the capacitance network of the cell.	e memory [F]
C_{dep}	Channel depletion capacitance of the memory transistor.	$[\mathbf{F}]$
C_{FG}	Overall capacitance of the floating gate.	$[\mathbf{F}]$
C_i	Capacitance between the node i and the floating gate node.	$[\mathbf{F}]$
$C_{[S,D,TD,CD]}$	Capacitance of the capacitors built by source, drain, tunnel and coupling dielectric, respectively.	dielectric [F]
C_{wl}	Overall word line capacitance.	$[\mathbf{F}]$
d	Distance between two memory transistors.	[cm]
$\delta(x)$	Dirac delta function.	
d_{TD}	Physical thickness of the tunnel dielectric.	[cm]
ε	Electric field.	$\left[MV_{/cm} ight]$
E_{CB}	Bottom level of the conduction band.	[eV]
E_F	Fermi level.	[eV]
ϵ_{ox}	Permittivity of silicon oxide $= 3.45 \cdot 10^{-13}$	$\begin{bmatrix} \mathbf{F}_{/\mathbf{cm}} \end{bmatrix}$
$\epsilon_{r,m}$	Relative dielectric permittivity of material m.	
ϵ_{Si}	Permittivity of silicon = $1.04 \cdot 10^{-12}$	$\left[\mathbf{F}_{\mathbf{/cm}} \right]$

Abbreviations and Symbols

f_{PV}	Verify function in the model of programmed V_{th} distribution	1.
γ_i	cross coupling ratio: Ratio of the strey capacitance to the <i>it</i> memory cell.	h adjacent [F]
$\gamma_{[diag,wl,bl,ch]}$	Cross coupling ratio to adjacent cell along the diagonal direline direction, bit line direction and to the adjacent channe tively.	ction, word 1el, respec-
g_m	Transconductance of the cell in the NAND string.	$\left[V_{/decade} \right]$
h	Plank constant.	$[{\bf J}\cdot{\bf s}]$
H(x)	Heavyside function in the model of programmed V_{th} distribution	ution.
\hbar	Reduced Plank constant, ($h/2\pi$).	$[{\bf J}\cdot{\bf s}]$
I_{ref}	Reference current in current sensing schemes.	[A]
I_{string}	Current flowing through the NAND string.	[A]
J_{FN}	Current density of the Fowler-Nordheim tunneling current	$\left[A_{cm^{2}} \right]$
k	Boltzmann Constant = $1.38 \cdot 10^{-23}$	$\begin{bmatrix} \mathbf{J}/\mathbf{K} \end{bmatrix}$
L(x)	Linear verify function in the model of programmed $V_{th}\ensuremath{\operatorname{dist}}$	ribution.
$L_{\rm MOS}$	Length of the MOS transistor.	[nm]
m^*	Electron effective mass in barrier material.	[kg]
μ	Mean Voltage value of the distribution.	$[\mathbf{V}]$
μ_e	Mean number of the distribution of electrons.	
μ_{eff}	Effective charge carrier mobility.	$\left[cm^{2}/Vs ight]$
N	Ensemble size of cells = Overall number of cells.	
N_a	Acceptor impurity concentration.	$\left[\mathrm{cm}^{-3} ight]$
n_e	Number of stored electrons.	
Δn_e	Number of tunneled electrons.	
N_{pp}	Minimal number of program pulses required to shift the V tion across the program verify level.	_{th} distribu-
$n(V_{th})$	Number of cells in a voltage intervall arround V_{th} .	
$pdf_{\mu,\sigma}$	Probability density function with the distribution parameter	ers μ and σ .

xii	Abbreviations and S	ymbols
Φ_B	Energy height of a potential barrier in the device's band structure	ucture. [eV]
pp	Overall number of program pulses in incremental step pulse proming schemes.	ogram-
$Pr(V_{th})$	Probability of a cell to have the threshold voltage V_{th} .	
ψ_B	Fermi level from intrinsic Fermi level.	$[\mathbf{V}]$
ψ_{FG}	Floating gate potential.	$[\mathbf{V}]$
ψ_i	Potential of the node <i>i</i> .	[V]
$\psi_{[S,D,ch,CG]}$	Potential of the nodes source, drain, channel and control gate, a tively.	respec- [V]
q	Elementary charge $= 1.60 \cdot 10^{-19}$	$[\mathbf{C}]$
Q_{FG}	Overall charge on the floating gate capacitor.	$[\mathbf{C}]$
δQ_i	Partial charge at the node i of the floating gate capacitor.	$[\mathbf{C}]$
R_{SL}	Series resistance of source line.	$[\Omega]$
R_{string}	Series resistance of the unselected cells of a NAND string.	$[\Omega]$
S	Describes the <i>s</i> th Program step in incremental step pulse proming schemes.	ogram-
σ	Standard deviation of the distribution.	$[\mathbf{V}]$
$\sigma_{\Delta V th}$	Standard deviation of the cells' V_{th} shift.	$[\mathbf{V}]$
σ_e	Standard deviation of the distribution of electrons.	
S_L	Number of cells in the NAND string.	
T	Temperature.	$[\mathbf{K}]$
t	Time.	$[\mathbf{s}]$
$t_{discharge}$	Duration of the discharge phase in voltage sensing schemes.	$[\mathbf{s}]$
t_{eff}	Effective barrier thickness	
V	Applied voltage.	$[\mathbf{V}]$
V_{bi}	Built-in junction voltage of a diode.	$[\mathbf{V}]$
V_{BL}	Established voltage on the bit line capacitor.	$[\mathbf{V}]$
V_{bpass}	Boosting voltage in self boosted negative threshold sensing.	$[\mathbf{V}]$

V_{cc}	Voltage of the common collector.	$\left[V \right]$
V_{ch}	Channel potential.	$\left[V \right]$
ΔV_{ch}	Boosted channel potential in self boosted program inhibit scheme.	$\left[V \right]$
V_{FB}	Flatband voltage of the MOSFET structure.	$\left[V \right]$
V_i	Potential difference between the potential of node i and the float gate potential.	ing [V]
V_{inhb}	Voltage applied to the bit line in weak programming schemes, trigg ing a minor program inhibit state.	ger- [V]
V_{pp}	Voltage applied to the word line of the selected page during program	. [V]
V_{ppass}	Voltage applied to the unselected word lines in a block during the p gram operation.	oro- [V]
$V_{precharge}$	Voltage level to which the bit line is precharged in the beginning or read or programm operation.	of a [V]
V_{read}	Voltage applied to the selected word lines in a block during the reoperation to evaluate the cell state.	ead [V]
ΔV_{read}	Voltage increment of V_{read} in cells' V_{th} sector scan.	[V]
V_{ref}	Reference voltage in voltage sensing schemes.	[A]
V_{rpass}	Voltage applied to the unselected word lines in a block during the reoperation.	ead [V]
V_{step}	Voltage increment by which V_{pp} is increased with each program put in incremental step puls programming.	ılse [V]
ΔV_{step}	Increase of V_{step} due to cross coupling to the neighbouring channel d ing inhibit of ABL schemes.	lur- [V]
V_{th}	Threshold voltage of a memory cell, which represents the stored in mation.	for- [V]
$V_{th,0}$	Native threshold voltage of a cell holding no stored charges.	[V]
$\Delta V_{th,cc}$	Threshold voltage shift caused by the cross coupling effect with ad cent memory cells.	lja- [V]
ΔV_{th}	Threshold voltage shift of the memory transistor.	[V]
$\Delta_{Vth,i}$	Threshold voltage shift on the i th adjacent memory cell.	[V]
$\Delta V_{th,in}$	Threshold voltage shift of the memory cell caused by injected charge	ges. [V]

$V_{th,init}$	Initial threshold voltage of the memory cell before programming p	ulse. [V]
V_{th}^{MOS}	Threshold voltage of the MOS transistor.	[V]
V_{th}^*	Cell's sensed threshold voltage.	[V]
V_{weak}	Voltage applied to the bitline in weak programming schemes, triping a minor program inhibit state.	gger- [V]
W	Intrinsic minimal distribution width of the cell's V_{th} distribution.	[V]
W_{MOS}	Width of the MOS transistor.	[nm]
W_{target}	Target width of the programmed V_{th} distribution.	[V]

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