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Control of Harmful Effects during the Program Operation in NAND Flash Memories

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Meiner Familie

"I may not have gone where I intended to go,
but I think I have ended up where I needed to be."
Douglas Adams

Abstract

The dissertation on hand presents research on NAND flash memories, which are the most recent of today's dominant memory technologies. Its market growth fueled the cut of its product cycles to about one year and also led to increasing diversity of NAND flash products. Both make the evolutionary research and development strategy difficult to handle. Therefore, it is in urgent need to evaluate the interactions of design and technology as well as the impact of intrinsic variations and of growing harmful effects on the cells' stored information as soon as possible in the development phase of the flash memory system. However, this requires models for cell - system interaction, which are able to link the physical and electrical properties of the memory transistors with the behavior of the memory system to support the systematic decision on trade offs.

For this purpose, this work discusses the cell physics of the non-volatile semiconductor memory cell as well as its write mechanisms. The direct interaction between the programming algorithm and physical cell parameters is investigated. The NAND memory array architecture and its implications on cells' read and program operations are presented. Harmful effects on the stored information are presented, categorized, analyzed, and for this purpose conceptually separated in disturb and noise effects. Algorithmic countermeasures for floating gate cross coupling, which was seen as major blocking point for future scaling, are proposed. It is shown by worst case analysis, that floating gate cross coupling can be efficiently controlled by algorithmic countermeasures.

Taking other harmful effects into account requires a more general and versatile analysis approach. Therefore a stochastic model for the program operation is derived and experimentally verified at 48 nm ground rule. The utility and flexibility of this model is demonstrated by discussing the control of cells' V_{th} by a weak programming strategy, and by the optimization of the transistor geometry for increased V_{th} control, respectively. This improved control may be used in future NAND flash memories to either improve the memory reliability or to increase the stored data density according to the requirements of the targeted application.

By including more and more of the previously discussed harmful effects into the model for cell-system interaction, it could mature to a complete NAND memory simulator. This dissertation demonstrates the feasibility of such an approach and establishes the theoretical foundations.

Contents

Abbreviations and Symbols

Abbreviations

16LC	16 Level Cell
8LC	8 Level Cell
AA	Active Area
AGL	Array Ground Line
BL	Bit Line
BPD	Background Pattern Dependency
BSEL	Block SElector Lines
BTBHH	Band To Band Hot Hole
CC	Cross Coupling
CD	Coupling Dielectric
CG	Control Gate
CHE	Channel Hot Electron
CTF	Charge Trapping Flash
DRAM	Dynamic Random Access Memory
ECC	Error Correcting Code
EEPROM	Electrical Erasable Programmable ROM
EOT	Equivalent Oxide Thickness
EPROM	Erasable Programmable ROM
ETOX	Erase Through OXide
F	minimal feature size

FETMOS	Floating-gate Electron Tunneling MOS
FG	Floating Gate
FLOTOX	FLOating-gate Tunneling OXide
FN	Fowler Nordheim
GP	Gate Plugs
GSL	Ground Select Line
GWL	Global Word Lines
HDD	Hard Disk Drives
IC	Integrated Circuit
IPD	Inter Poly Dielectric
ISPP	Incremental Step Pulse Programming
ITRS	International Technology Roadmap for Semiconductors
IWD	Inter Word line Dielectric
LRD	Local Row Decoder
LSB	Least Significant Bit
MC	Monte-Carlo
MLC	Multi Level Cell
MNOS	Metal Nitride Oxide Seminconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NOP	Number Of Programs
NVM	Non-Volatile Memory
NVSM	Non-Volatile Semiconductor Memory
OTP	One Time Programmable
PAE	Program After Erase
PROM	Programmable-ROM
PV	Program Verify

PW	Program Weak
RAM	Random Access Memory
ROM	Read Only Memory
RTN	Random Telegraph noise
SA-STI	Self Aligned-Shallow Trench Isolation
SBEI	Self Boosted Erase Inhibit
SBNV	Self Boosted Negative Verify
SBPI	Self Boosted Program Inhibit
SL	Source Line
SLN	Source Line Noise
SOI	Silicon On Insulator
SONOS	Silicon-Oxide-Nitride-Oxide-Silicon
SRAM	Static RAM
SSD	Solid State Disk
SSL	String Select Line
STI	Shallow Trench Isolation
TD	Tunneling Dielectric
WL	Word Line

Symbols

$\star$	Convolution	
$A_{cc,i}$	Area facing the ith adjacent cell.	$[\mathrm{cm}^2]$
α	Gate coupling ratio of the capacitance of the coupling dielectric to the overall floating gate capacitance.	
α_{cc}	Word line coupling ratio of the inter word line capacitance and the word line capacitance.	
AR	Accuracy Range parameter of verify functions in the model of programmed V_{th} distributions.	[V]
b	Number of bits stored in a single memory cell.	
C_{BL}	Overall bit line capacitance.	[F]
C_{cell}	Simplified cell capacitance of the capacitance network of the memory cell.	[F]
C_{dep}	Channel depletion capacitance of the memory transistor.	[F]
C_{FG}	Overall capacitance of the floating gate.	[F]
C_i	Capacitance between the node i and the floating gate node.	[F]
$C_{[S,D,TD,CD]}$	Capacitance of the capacitors built by source, drain, tunnel dielectric and coupling dielectric, respectively.	[F]
C_{wl}	Overall word line capacitance.	[F]
d	Distance between two memory transistors.	[cm]
$\delta(x)$	Dirac delta function.	
d_{TD}	Physical thickness of the tunnel dielectric.	[cm]
$\mathcal{E}$	Electric field.	$\left[\mathrm{MV/cm}\right]$
E_{CB}	Bottom level of the conduction band.	[eV]
E_F	Fermi level.	[eV]
ϵ_{ox}	Permittivity of silicon oxide $= 3.45 \cdot 10^{-13}$	$\left[\mathrm{F/cm}\right]$
$\epsilon_{r,m}$	Relative dielectric permittivity of material m.	
ϵ_{Si}	Permittivity of silicon $= 1.04 \cdot 10^{-12}$	$\left[\mathrm{F/cm}\right]$

f_{PV}	Verify function in the model of programmed V_{th} distribution.	
γ_i	cross coupling ratio: Ratio of the strey capacitance to the ith adjacent memory cell.	$[\mathrm{F}]$
$\gamma_{[diag,wl,bl,ch]}$	Cross coupling ratio to adjacent cell along the diagonal direction, word line direction, bit line direction and to the adjacent channel, respectively.	
g_m	Transconductance of the cell in the NAND string.	$\left[\mathrm{V/decade}\right]$
h	Plank constant.	$[\mathrm{J \cdot s}]$
$H(x)$	Heavyside function in the model of programmed V_{th} distribution.	
$\hbar$	Reduced Plank constant, $(h/2\pi)$.	$[\mathrm{J \cdot s}]$
I_{ref}	Reference current in current sensing schemes.	$[\mathrm{A}]$
I_{string}	Current flowing through the NAND string.	$[\mathrm{A}]$
J_{FN}	Current density of the Fowler-Nordheim tunneling current.	$\left[\mathrm{A/cm^2}\right]$
k	Boltzmann Constant $= 1.38 \cdot 10^{-23}$	$\left[\mathrm{J/K}\right]$
$L(x)$	Linear verify function in the model of programmed V_{th} distribution.	
L_{MOS}	Length of the MOS transistor.	$[\mathrm{nm}]$
m^*	Electron effective mass in barrier material.	$[\mathrm{kg}]$
μ	Mean Voltage value of the distribution.	$[\mathrm{V}]$
μ_e	Mean number of the distribution of electrons.	
μ_{eff}	Effective charge carrier mobility.	$\left[\mathrm{cm^2/Vs}\right]$
N	Ensemble size of cells = Overall number of cells.	
N_a	Acceptor impurity concentration.	$\left[\mathrm{cm^{-3}}\right]$
n_e	Number of stored electrons.	
Δn_e	Number of tunneled electrons.	
N_{pp}	Minimal number of program pulses required to shift the V_{th} distribution across the program verify level.	
$n(V_{th})$	Number of cells in a voltage intervall arround V_{th}.	
$pdf_{\mu,\sigma}$	Probability density function with the distribution parameters μ and σ.	

Φ_B	Energy height of a potential barrier in the device's band structure.	[eV]
pp	Overall number of program pulses in incremental step pulse programming schemes.	
$Pr(V_{th})$	Probability of a cell to have the threshold voltage V_{th}.	
ψ_B	Fermi level from intrinsic Fermi level.	[V]
ψ_{FG}	Floating gate potential.	[V]
ψ_i	Potential of the node i.	[V]
$\psi_{[S,D,ch,CG]}$	Potential of the nodes source, drain, channel and control gate, respectively.	[V]
q	Elementary charge $= 1.60 \cdot 10^{-19}$	[C]
Q_{FG}	Overall charge on the floating gate capacitor.	[C]
δQ_i	Partial charge at the node i of the floating gate capacitor.	[C]
R_{SL}	Series resistance of source line.	[Ω]
R_{string}	Series resistance of the unselected cells of a NAND string.	[Ω]
s	Describes the sth Program step in incremental step pulse programming schemes.	
σ	Standard deviation of the distribution.	[V]
$\sigma_{\Delta Vth}$	Standard deviation of the cells' V_{th} shift.	[V]
σ_e	Standard deviation of the distribution of electrons.	
S_L	Number of cells in the NAND string.	
T	Temperature.	[K]
t	Time.	[s]
$t_{discharge}$	Duration of the discharge phase in voltage sensing schemes.	[s]
t_{eff}	Effective barrier thickness	
V	Applied voltage.	[V]
V_{bi}	Built-in junction voltage of a diode.	[V]
V_{BL}	Established voltage on the bit line capacitor.	[V]
V_{bpass}	Boosting voltage in self boosted negative threshold sensing.	[V]

V_{cc}	Voltage of the common collector.	[V]
V_{ch}	Channel potential.	[V]
ΔV_{ch}	Boosted channel potential in self boosted program inhibit scheme.	[V]
V_{FB}	Flatband voltage of the MOSFET structure.	[V]
V_i	Potential difference between the potential of node i and the floating gate potential.	[V]
V_{inhb}	Voltage applied to the bit line in weak programming schemes, triggering a minor program inhibit state.	[V]
V_{pp}	Voltage applied to the word line of the selected page during program.	[V]
V_{ppass}	Voltage applied to the unselected word lines in a block during the program operation.	[V]
$V_{precharge}$	Voltage level to which the bit line is precharged in the beginnging of a read or programm operation.	[V]
V_{read}	Voltage applied to the selected word lines in a block during the read operation to evaluate the cell state.	[V]
ΔV_{read}	Voltage increment of V_{read} in cells' V_{th} sector scan.	[V]
V_{ref}	Reference voltage in voltage sensing schemes.	[A]
V_{rpass}	Voltage applied to the unselected word lines in a block during the read operation.	[V]
V_{step}	Voltage increment by which V_{pp} is increased with each program pulse in incremental step puls programming.	[V]
ΔV_{step}	Increase of V_{step} due to cross coupling to the neighbouring channel during inhibit of ABL schemes.	[V]
V_{th}	Threshold voltage of a memory cell, which represents the stored information.	[V]
$V_{th,0}$	Native threshold voltage of a cell holding no stored charges.	[V]
$\Delta V_{th,cc}$	Threshold voltage shift caused by the cross coupling effect with adjacent memory cells.	[V]
ΔV_{th}	Threshold voltage shift of the memory transistor.	[V]
$\Delta_{Vth,i}$	Threshold voltage shift on the ith adjacent memory cell.	[V]
$\Delta V_{th,in}$	Threshold voltage shift of the memory cell caused by injected charges.	[V]

$V_{th,init}$	Initial threshold voltage of the memory cell before programming pulse.	[V]
V_{th}^{MOS}	Threshold voltage of the MOS transistor.	[V]
V_{th}^{*}	Cell's sensed threshold voltage.	[V]
V_{weak}	Voltage applied to the bitline in weak programming schemes, triggering a minor program inhibit state.	[V]
W	Intrinsic minimal distribution width of the cell's V_{th} distribution.	[V]
W_{MOS}	Width of the MOS transistor.	[nm]
W_{target}	Target width of the programmed V_{th} distribution.	[V]

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