

Lehrstuhl für Technische Elektronik
der Technischen Universität München

Parametric Reliability of 6T-SRAM Core Cell Arrays

Stefan Drapatz

Vollständiger Abdruck der von der Fakultät für Elektrotechnik und Informationstechnik
der Technischen Universität München zur Erlangung des akademischen Grades eines

Doktor-Ingenieurs

genehmigten Dissertation.

Vorsitzender: Univ.-Prof. Dr.-Ing. Georg Sigl

Prüfer der Dissertation:

1. Univ.-Prof. Dr. rer. nat. Doris Schmitt-Landsiedel
2. apl. Prof. Dr.-Ing. habil. Walter Stechele

Die Dissertation wurde am 14.10.2011 bei der Technischen Universität München eingereicht und durch die Fakultät für Elektrotechnik und Informationstechnik am 7.02.2012 angenommen.

Selected Topics of Electronics and Micromechatronics
Ausgewählte Probleme der Elektronik und Mikromechatronik

Volume 43

Stefan Drapatz

Parametric Reliability of 6T-SRAM Core Cell Arrays

Shaker Verlag
Aachen 2012

Bibliographic information published by the Deutsche Nationalbibliothek

The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available in the Internet at <http://dnb.d-nb.de>.

Zugl.: München, Techn. Univ., Diss., 2012

Copyright Shaker Verlag 2012

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior permission of the publishers.

Printed in Germany.

ISBN 978-3-8440-1009-1

ISSN 1618-7539

Shaker Verlag GmbH • P.O. BOX 101818 • D-52018 Aachen

Phone: 0049/2407/9596-0 • Telefax: 0049/2407/9596-9

Internet: www.shaker.de • e-mail: info@shaker.de

Summary

The increasing integration density of microelectronic circuits in combination with non-constantly scaled supply voltages results in higher electric fields in MOS transistors. This is one central source of several aging mechanisms, some of them shifting the parameters of MOS transistors during lifetime. These parametric degradation effects can be separated in two groups called 'Bias Temperature Instability' (BTI) and 'Hot Carrier Injection' (HCI). This work focuses on the impact of these degradation mechanisms on 6-Transistor Static Random Access Memory (SRAM) arrays in 65 nm low power CMOS technology.

First, some basic information is provided about SRAM cell functionality, key performance metrics, reliability and the four parametric degradation mechanisms covered in this work. Then, the sensitivity of the SRAM core cell to each degradation mechanism is simulated. Together with the effective device degradation under normal SRAM operations in real life, this results in the information about the impact of each mechanism. BTI for pMOS transistors, called Negative BTI (NBTI), could be identified as the main problem in actual 65 nm low power technology with conventional SiO_2 gate dielectrics.

NBTI shows strong variation- and recovery-effects, which both are not fully understood, although this degradation mechanism has been known for approx. 30 years. This is why there are no sufficient simulation models so far, thus, measurements have to be performed to do the step from single cell simulation to SRAM array conclusions.

Consequently, a major focus of this work is to develop unconventional new measurement techniques. Contrary to state-of-the-art methods they are faster, do not need dedicated test chips which do not represent mass product design, do not need highly accurate V-I measurements and therefore can be used in-field in products with the only precondition of dual- V_{DD} power routing.

By using these new techniques, the impact of the worst degradation mechanism NBTI was examined directly on large-scale SRAM arrays. Especially the fast-recovering component of NBTI was directly measured on SRAM array stability for the first time. Thus, it could be shown which use-cases are critical to provide long lifetimes, which is the first step to fight the impact of parametric degradation mechanisms.

Finally, a comparison of known countermeasure techniques was performed in order to choose the most promising methods.

Contents

Summary	i
I Introduction and Background	1
1 Introduction	3
1.1 Technology Scaling: Benefits and Challenges	4
1.2 Scaling of SRAM: Motivation for this work	5
1.3 Outline and Contributions of this work	6
2 SRAM Fundamentals	7
2.1 Functionality of the 6T-SRAM Core Cell	9
2.2 SRAM Performances and Figures of Merit	10
2.3 Summary	19
3 Degradation and Reliability	21
3.1 Quality, Yield, Variations and Redundancy	21
3.2 Reliability Basics	22
3.3 Physics-of-Failure Concept	25
3.4 Parametrical Degradation Mechanisms	26
3.5 Negative Bias Temperature Instability (NBTI)	28
3.6 Positive Bias Temperature Instability (PBTI)	33
3.7 Hot Carrier Injection (HCI) and Non-conducting HCI (NCHCI)	35
3.8 Accelerated Stress Measurements	38
3.9 Summary	39

II	Parametric Degradations on 6T-SRAM Core Cells	41
4	Simulations of the four Parametric Degradation Mechanisms	43
4.1	Voltage and Current in each Transistor	43
4.2	Negative Bias Temperature Instability	53
4.3	Positive Bias Temperature Instability	56
4.4	Hot Carrier Injection	63
4.5	Off-State Stress	68
4.6	NBTI plus PBTI	69
4.7	Conclusion	73
5	Stability Analysis of SRAM Arrays	75
5.1	State of the Art: SRAM Stability Analysis	75
5.2	New Approach	76
5.3	Simulation of Read Margin	76
5.4	Experimental setup	80
5.5	Results	84
5.6	Discussion	90
5.7	Conclusion	91
6	Impact of Recovering NBTI on SRAM Arrays	93
6.1	State of the Art: Measure Recovering NBTI on SRAM Cells	93
6.2	New Approach	96
6.3	Results	101
6.4	Plausibility checks	103
6.5	Temperature dependency of NBTI recovery	110
6.6	Determination of Read Margin Distribution directly after end of Stress . . .	111
6.7	Conclusion	113
III	Countermeasures	115
7	Countermeasures	117
7.1	The different levels of countermeasures	117
7.2	Countermeasures against instability	118

7.3	Countermeasures against NBTI- and PBTI specific V_{th} drift	123
7.4	Comparison of countermeasure techniques	126
7.5	The best countermeasure techniques	127
7.6	Conclusion	130
8	Conclusion and Outlook	131
	Appendix	135
A	Determination of Static Noise Margin SNM and Read N-Curve	137
B	Determination of Read Margin RM	138
C	Determination of Write Level or Write-Trip Point	139
D	Determination of Write N-Curve	140
E	Determination of Read Current I_{read}	141
F	List of Symbols and Abbreviations	142
G	Publications by the author	144
	List of Figures	147
	Bibliography	155
	Danksagung	160