Lehrstuhl für Technische Elektronik
der Technischen Universität München

Parametric Reliability of 6T-SRAM Core Cell Arrays

Stefan Drapatz

Vollständiger Abdruck der von der Fakultät für Elektrotechnik und Informationstechnik der Technischen Universität München zur Erlangung des akademischen Grades eines

Doktor-Ingenieurs

genehmigten Dissertation.

Vorsitzender: Univ.-Prof. Dr.-Ing. Georg Sigl

Prüfer der Dissertation:

1. Univ.-Prof. Dr. rer. nat. Doris Schmitt-Landsiedel
2. apl. Prof. Dr.-Ing. habil. Walter Stechele

Die Dissertation wurde am 14.10.2011 bei der Technischen Universität München eingereicht und durch die Fakultät für Elektrotechnik und Informationstechnik am 7.02.2012 angenommen.

Selected Topics of Electronics and Micromechatronics
Ausgewählte Probleme der Elektronik und Mikromechatronik

Volume 43

Stefan Drapatz

Parametric Reliability of 6T-SRAM Core Cell Arrays

Shaker Verlag
Aachen 2012

Bibliographic information published by the Deutsche Nationalbibliothek
The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available in the Internet at http://dnb.d-nb.de.

Zugl.: München, Techn. Univ., Diss., 2012

Printed in Germany.

ISBN 978-3-8440-1009-1
ISSN 1618-7539

Shaker Verlag GmbH • P.O. BOX 101818 • D-52018 Aachen
Phone: 0049/2407/9596-0 • Telefax: 0049/2407/9596-9
Internet: www.shaker.de • e-mail: info@shaker.de

Summary

The increasing integration density of microelectronic circuits in combination with non-constantly scaled supply voltages results in higher electric fields in MOS transistors. This is one central source of several aging mechanisms, some of them shifting the parameters of MOS transistors during lifetime. These parametric degradation effects can be separated in two groups called 'Bias Temperature Instability' (BTI) and 'Hot Carrier Injection' (HCI). This work focuses on the impact of these degradation mechansisms on 6-Transistor Static Random Access Memory (SRAM) arrays in 65 nm low power CMOS technology.

First, some basic information is provided about SRAM cell functionality, key performance metrics, reliability and the four parametric degradation mechanisms covered in this work. Then, the sensitivity of the SRAM core cell to each degradation mechanism is simulated. Together with the effective device degradation under normal SRAM operations in real life, this results in the information about the impact of each mechanism. BTI for pMOS transistors, called Negative BTI (NBTI), could be identified as the main problem in actual 65 nm low power technology with conventional SiO_2 gate dielectrics.

NBTI shows strong variation- and recovery-effects, which both are not fully understood, although this degradation mechanism has been known for approx. 30 years. This is why there are no sufficient simulation models so far, thus, measurements have to be performed to do the step from single cell simulation to SRAM array conclusions.
Consequently, a major focus of this work is to develop unconventional new measurement techniques. Contrary to state-of-the-art methods they are faster, do not need dedicated test chips which do not represent mass product design, do not need highly accurate V-I measurements and therefore can be used in-field in products with the only precondition of dual-V_{DD} power routing.
By using these new techniques, the impact of the worst degradation mechanism NBTI was examined directly on large-scale SRAM arrays. Especially the fast-recovering component of NBTI was directly measured on SRAM array stability for the first time. Thus, it could be shown which use-cases are critical to provide long lifetimes, which is the first step to fight the impact of parametric degradation mechanisms.
Finally, a comparison of known countermeasure techniques was performed in order to choose the most promising methods.

Contents