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Parametric Reliability of 6T-SRAM Core Cell Arrays

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Summary

The increasing integration density of microelectronic circuits in combination with non-constantly scaled supply voltages results in higher electric fields in MOS transistors. This is one central source of several aging mechanisms, some of them shifting the parameters of MOS transistors during lifetime. These parametric degradation effects can be separated in two groups called 'Bias Temperature Instability' (BTI) and 'Hot Carrier Injection' (HCI).

This work focuses on the impact of these degradation mechanisms on 6-Transistor Static Random Access Memory (SRAM) arrays in 65 nm low power CMOS technology.

First, some basic information is provided about SRAM cell functionality, key performance metrics, reliability and the four parametric degradation mechanisms covered in this work. Then, the sensitivity of the SRAM core cell to each degradation mechanism is simulated. Together with the effective device degradation under normal SRAM operations in real life, this results in the information about the impact of each mechanism. BTI for pMOS transistors, called Negative BTI (NBTI), could be identified as the main problem in actual 65 nm low power technology with conventional SiO₂ gate dielectrics.

NBTI shows strong variation- and recovery-effects, which both are not fully understood, although this degradation mechanism has been known for approx. 30 years. This is why there are no sufficient simulation models so far, thus, measurements have to be performed to do the step from single cell simulation to SRAM array conclusions.

Consequently, a major focus of this work is to develop unconventional new measurement techniques. Contrary to state-of-the-art methods they are faster, do not need dedicated test chips which do not represent mass product design, do not need highly accurate V-I-measurements and therefore can be used in-field in products with the only precondition of dual-VDD power routing.

By using these new techniques, the impact of the worst degradation mechanism NBTI was examined directly on large-scale SRAM arrays. Especially the fast-recovering component of NBTI was directly measured on SRAM array stability for the first time. Thus, it could be shown which use-cases are critical to provide long lifetimes, which is the first step to fight the impact of parametric degradation mechanisms.

Finally, a comparison of known countermeasure techniques was performed in order to choose the most promising methods.