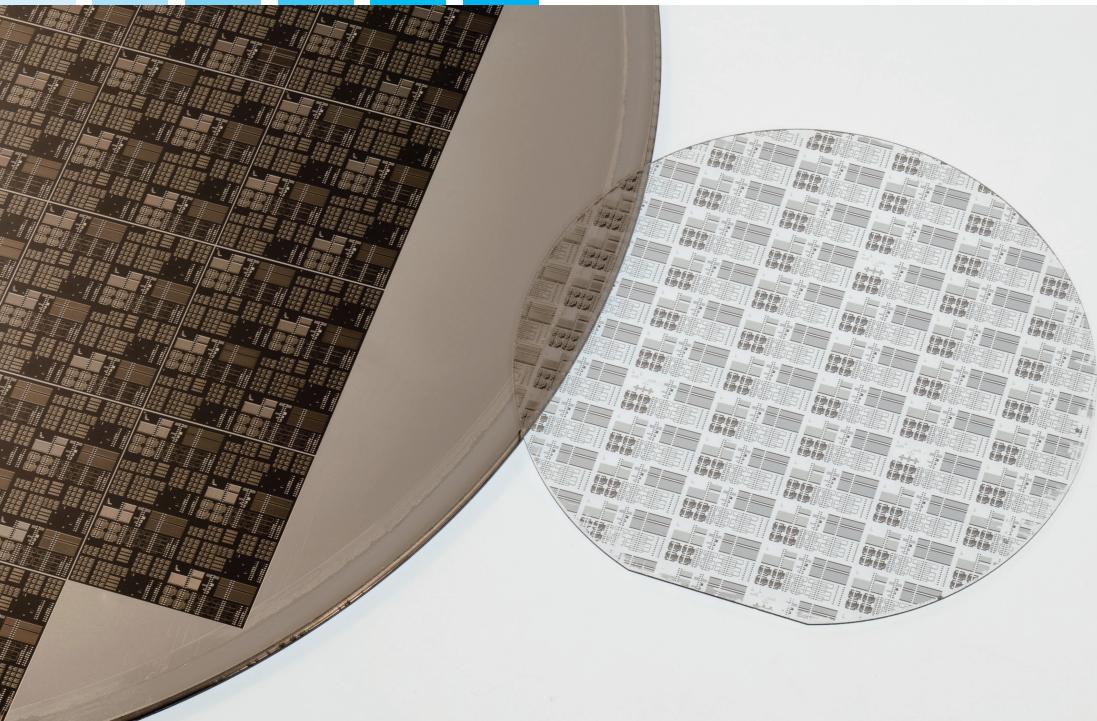


Gallium Nitride High Electron Mobility Transistors on Native Substrates for Power Switching Applications

Fabrication, Characterization and Modelling

Muhammad Alshahed



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Muhammad Alshahed

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Abstract

In this work, Gallium Nitride (GaN) HEMTs on native substrates are fabricated, characterised and modelled. The GaN-on-GaN HEMTs feature an off-state leakage current three orders of magnitude lower than GaN HEMTs on Silicon and Sapphire substrates. In addition, the GaN-on-GaN HEMTs exhibit a current collapse of less than 15 %, which is significantly lower than the values measured for GaN-on-Si HEMTs and GaN-on-Sapphire HEMTs of 35 % and 60 % respectively for the same operational conditions. The superior electrical characteristics of GaN-on-GaN HEMTs are correlated to the significantly lower density of structural imperfections, such as threading dislocations, which increase the parasitic leakage current and act as trapping centres for electrons. Unlike what has been reported in previous literature studies that a compromise has to be made between the leakage current and the dynamic on-resistance of the GaN HEMTs, in this work we show that this is only true if there exists a high density of trapping centers, such as threading dislocations and compensation doping species, and a simultaneous high density of free carriers, either through unintentional doping species or by carrier conduction through dislocations. In the case of GaN-on-GaN, TEM analyses reveal a defect density below 10^6 cm^{-2} in comparison to $2.7 \times 10^9 \text{ cm}^{-2}$ for GaN-on-Si and $9 \times 10^8 \text{ cm}^{-2}$ for GaN-on-Sapphire. This low defect density combined with the low leakage current lead to a pulsed drain current that is more robust against high voltage stress bias.

A compact physics-based HEMT model that captures the dynamic effects of charge trapping and emission during high voltage switching has been developed in Verilog-A format. The memory effect of the charge trapping and emission in GaN HEMTs subjected to stress bias is implemented in the form of a finite state machine. By including the signatures of the dominant trapping species in the model, the simulation results are in excellent agreement with the measurement results. The off-state leakage current is also captured in the model, which is divided into a linear (ohmic) and a non-linear (space-charge-limited) leakage current, that matches the measured leakage current with high reproducibility on the whole wafer and from wafer to wafer. The HEMT model is an electro-thermal model that captures the self-heating given the right parameters of the thermal sub-circuit. The extraction methodology of the thermal circuit parameters is developed on a measurement-based foundation and is verified for different packaging technologies and operation conditions.

The significantly lower defect density in the case of GaN-on-GaN leads to an improvement, as well, in the thermal conductivity of the HEMTs. For GaN on foreign substrates, the lattice and thermal mismatches, as well as the need for multiple epitaxial layers for strain relief and compensation doping, lead to a degradation of the thermal conductivity through

the material. This poor thermal conductivity is partially a result of phonon scattering at the interfaces and the defective sites. Therefore, in GaN-on-GaN, even with the identical epitaxial layers structure as that for GaN-on-Si and GaN-on-Sapphire, the drain current drop due to self-heating is less than 2 % in comparison to 8 % to 15 % for GaN-on-Sapphire and 9 % to 13 % in the case of GaN-on-Si. The conclusion about the effect of dislocations on the thermal conductivity is deduced from the experiment where the Si substrate is thinned down to 44 μm , which results in only a slight improvement of the overall thermal conductivity of the GaN-on-Si HEMTs. However, by completely removing the Si substrate and transferring the GaN epitaxial layers to another Si carrier by means of metal bonding, the thermal conductivity of the transferred layers approached that of the GaN-on-GaN HEMTs.

Keywords:

bulk GaN, compact modelling, current collapse, dynamic R_{on} , GaN HEMT, leakage currents, measurement-based thermal modelling, power semiconductor devices, Power transistors, self-heating, semiconductor device reliability, threading dislocations, thermal power dissipation, thermal resistance, thermal transfer function.

Kurzfassung

Diese Arbeit beschreibt die Herstellung, Charakterisierung und Modellierung von Gallium-Nitrid (GaN) HEMTs auf nativen Substraten. Die nativen GaN HEMTs weisen um drei Größenordnungen niedrigere Leckströme als die von GaN HEMTs auf Silizium- und Saphirsubstraten auf. Außerdem, zeigen die nativen HEMTs eine Stromdispersion von weniger als 15 % im Vergleich zu 35 % im Fall von GaN auf Silizium und 60 % im Fall von GaN auf Saphir für die gleichen Betriebsbedingungen. Die ausgezeichneten elektrischen Eigenschaften der nativen GaN HEMTs sind mit der deutlich geringeren Dichte an Kristallfehlern, zum Beispiel Stufenversetzungen und Schraubenversetzungen, korreliert. Solche Kristallfehler verursachen höhere parasitäre Leckströme und wirken gleichzeitig als Elektronenfangstellen. Gemäß früheren Literaturstudien muss ein Kompromiss zwischen dem Leckstrom und dem Durchgangswiderstand (R_{on}) gesucht werden. Dennoch wird in dieser Arbeit gezeigt, dass dieser Kompromiss nur dann gesucht werden kann, wenn sowohl eine hohe Dichte an beweglichen Ladungsträgern, entweder aus der Hintergrunddotierung oder über Leckströme durch Fadenversetzungen verursacht, als auch eine hohe Dichte von Elektronenfangstellen, wie durch Kompensationsdotierung und Defekte, gleichzeitig vorhanden sind. Transmissionselektronenmikroskopie-Analysen zeigen eine Defektdichte von weniger als 10^6 cm^{-2} für native GaN HEMTs im Vergleich zu $2.7 \times 10^9 \text{ cm}^{-2}$ für GaN auf Silizium und $9 \times 10^8 \text{ cm}^{-2}$ für GaN auf Saphir HEMTs. Kombiniert mit einem geringen Leckstrom bewirkt diese niedrige Defektdichte einen robusten gepulsten Drainstrom bei hoher Spanungsbelastung im Sperrzustand.

Ein kompaktes physikalisches GaN HEMT Modell, das die dynamischen Effekte des Einfangens und der Emission von Ladungen bei Hochspannungsschaltvorgängen beschreiben kann, wird in Verilog-A Format entwickelt. Ein endlicher Zustandsautomat beschreibt den Gedächtniseffekt des Einfangens und der Emission der Ladungen in GaN HEMTs unter Stressbias. Die Simulationsergebnisse stimmen dann genau mit den Messungsergebnissen überein, wenn die charakterisierenden Eigenschaften der dominanten Fangstellen ins Modell einbezogen werden. Der Leckstrom im Sperrzustand des GaN HEMTs ist ebenfalls im Modell erfasst, wobei er in einen linearen (ohmschen) und einen nichtlinearen (raumladungsbeschränkten) Bereich unterteilt wird. Vorausgesetzt, dass die richtigen Parameter der thermischen Schaltung angegeben sind, kann das elektrothermische Modell die Selbsterwärmung des GaN HEMTs beschreiben. Die Extraktionsmethode der Parameter der thermischen Schaltung ist auf einer messbasierten Grundlage entwickelt und wurde für verschiedene Aufbautechniken und Betriebsbedingungen überprüft.

Die deutlich geringere Defektdichte des nativen GaN HEMTs verbessert die thermische Leitfähigkeit des Transistors. Für GaN HEMTs auf Fremdsubstraten führen die geringere thermische Leitfähigkeit und die Gitterfehlanpassungen sowie die Notwendigkeit des Einbringens mehrerer Stress-Kompensationsschichten zu einer Verschlechterung der thermischen Leitfähigkeit des Materials. Die schlechte thermische Leitfähigkeit ist teilweise von Phononen-Streuung an Schnittstellen und Defektstellen verursacht. Daher weist der native GaN HEMT mit gleichen epitaktischen Schichtstrukturen wie für GaN auf Silizium und GaN auf Saphir einen Abfall des Drainstroms aufgrund von Selbsterwärmung von weniger als 2 % im Vergleich zu 8 % - 15 % für GaN auf Saphir und 9 % - 13 % für GaN auf Si auf. In einem Experiment, wo der Si-Substrat auf $44 \mu\text{m}$ rückgedünnt wurde, ergibt sich eine minimale Verbesserung der gesamten thermischen Leitfähigkeit des GaN HEMTs, was die Auswirkung der Fadenversetzungen auf die thermische Leitfähigkeit bestätigt. Jedoch nähert sich nach der vollständigen Entfernung des Silizium-Substrats von einem Wafer mit GaN auf Si HEMTs und der erfolgreichen Übertragung der epitaktischen Schichten auf ein Trägersubstrat mittels Metallbindung die thermische Leitfähigkeit der übergetragenen Schichten von nativen GaN HEMTs an.

Schlagwörter:

dynamische R_{on} , Fadenversetzungen, GaN HEMT, Halbleiter Zuverlässigkeit, kompakt Modellierung, Leckströme, Leistungshalbleiter, Leistungstransistor, messbasierende thermische Modellierung, nativ GaN, Selbsterwärmung, Stromdispersion, thermische Übertragungsfunktion, thermische Verlustleistung, thermische Widerstand.

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Wir sind für nichts so dankbar wie für
Dankbarkeit

Marie Freifrau von Ebner-Eschenbach
(1830 - 1916)

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List of Abbreviations

<i>2DEG</i>	Two Dimensional Electron Gas
<i>AC</i>	Alternating Current
<i>Al</i>	Aluminium
<i>AlGaN</i>	Aluminium Gallium Nitride
<i>AlN</i>	Aluminium Nitride
<i>AlSiCu</i>	Aluminium Silicon Copper Alloy
<i>Au</i>	Gold
<i>BFOM</i>	Baliga Figure of Merit
<i>BFTEM</i>	Bright Field Transmission Electron Microscopy
<i>C – GaN</i>	Compensation-doped GaN
<i>CTE</i>	Coefficient of Thermal Expansion
<i>D – Mode</i>	Depletion Mode
<i>DC</i>	Direct Current
<i>DFTEM</i>	Dark Field Transmission Electron Microscopy
<i>E – beam</i>	Electron Beam
<i>E – Mode</i>	Enhancement Mode
<i>EDX</i>	Energy Dispersive X-Ray Spectroscopy
<i>FOM</i>	Figure of Merit

<i>FSM</i>	Finite-State Machine
<i>GaAs</i>	Gallium Arsenide
<i>GaN</i>	Gallium Nitride
<i>GaN/GaN</i>	GaN-on-GaN Substrate
<i>GaN/Sapphire</i>	GaN-on-Sapphire Substrate
<i>GaN/Si</i>	GaN-on-Silicon Substrate
<i>GPA</i>	Geometric Phase Analysis
<i>HAADF</i>	High Angle Annular Dark Field Imaging
<i>HCL</i>	Hydrochloric Acid
<i>HEMT</i>	High Electron Mobility Transistor
<i>HF</i>	Hydrofluoric acid
<i>HPNS</i>	High Pressure Nitrogen Solution
<i>HVPE</i>	Hydride Vapour Phase Epitaxy
<i>IGBT</i>	Insulated-Gate Bipolar Transistor
<i>JFOM</i>	Johnson Figure of Merit
<i>LPCVD</i>	Low Pressure Chemical Vapour Deposition
<i>MESFET</i>	Metal Semiconductor Field Effect Transistor
<i>MISHEMT</i>	Metal Insulator Semiconductor High Electron Mobility Transistor
<i>MIT – VSM</i>	Massachusetts Institute of Technology - Virtual Source Model
<i>MOCVD</i>	Metal Organic Chemical Vapour Deposition
<i>MOSFET</i>	Metal Oxide Semiconductor Field Effect Transistor
<i>Na – flux</i>	Sodium flux
<i>Ni</i>	Nickel
<i>PECVD</i>	Plasma Enhanced Chemical Vapour Deposition

<i>PF</i>	Poole-Frenkel
<i>R_{on}</i>	On-state Resistance
<i>RF</i>	Radio Frequency
<i>RIE</i>	reactive Ion Etching
<i>rms</i>	Root Mean Squared
<i>RMSE</i>	Root Mean Square Error
<i>SAED</i>	Selected Area Electron Diffraction
<i>sccm</i>	Standard Cubic Centimetre per minute
<i>SCLC</i>	Space Charge Limited Current
<i>SEM</i>	Scanning Electron Microscope
<i>Si</i>	Silicon
<i>Si₃N₄</i>	Silicon Nitride
<i>SiC</i>	Silicon Carbide
<i>SiO₂</i>	Silicon Oxide
<i>TBR</i>	Thermal Boundary resistance
<i>TCAD</i>	Technology Computer Aided Design
<i>TDD</i>	Threading Dislocation Density
<i>TEM</i>	Transmission Electron Microscopy
<i>Ti</i>	Titanium
<i>TMAH</i>	TetraMethyl Ammonium Hydroxide
<i>uid</i>	Unintentionally Doped
<i>V_{tfl}</i>	Trap Filling Level Voltage
<i>XRD</i>	X-Ray Diffraction

Contents

List of Abbreviations	x
List of Figures	xvi
List of Tables	xxx
1 Introduction	1
1.1 Motivation	1
1.2 Towards GaN power switches	5
2 Fundamentals and Background	8
2.1 GaN Material System	8
2.1.1 GaN Crystal Structure	8
2.1.2 The formation of the two-dimensional electron gas	10
2.2 General considerations of the GaN epitaxial material	15
2.2.1 Choice of substrates for GaN epitaxy	15
2.2.2 Typical structure of GaN epitaxial wafers	18
2.2.3 Challenges and prospects in the GaN epitaxy	19
2.3 Fabrication technology of GaN HEMTs	21
2.3.1 Conventional and CMOS compatible fabrication	21
2.3.2 Challenges in device fabrication	26
2.4 Operation Principle of GaN HEMTs	30
2.4.1 Current conduction in the 2DEG and gate modulation	30
2.4.2 GaN-specific non-idealities in device characteristics	32
3 Electrical characterization of GaN/Si HEMTs	35
3.1 Static Characteristics of GaN HEMTs	36
3.1.1 On-state GaN HEMT characteristics	36
3.1.2 Off-state GaN HEMT characteristics	38

3.2	Dynamic characteristics of GaN HEMTs	49
3.2.1	Trapping in the epitaxial buffer layers in DC power switching	49
3.2.2	Surface-related carrier trapping characterization using HEMTs with multiple secondary gates	54
3.3	Reliability issues of GaN/Si HEMTs	59
3.3.1	The role of threading dislocations in GaN epitaxial layers	60
3.3.2	Impact of threading dislocations on the structural and electrical properties of GaN/Si HEMTs	61
4	Electrical Modelling of GaN HEMTs	65
4.1	Case study: Feasibility of using GaN/Si HEMT in Instrumentation	66
4.1.1	Bidirectional power switch using GaN HEMT in cascode configuration	66
4.1.2	Bidirectional GaN HEMT cascode simulation results	68
4.2	Compact physical modelling of GaN HEMTs	72
4.2.1	Related previous modelling work	72
4.2.2	Proposed compact model derivation	73
4.2.3	Compact model Implementation in Verilog-A	80
4.2.4	Compact model validation	80
4.2.5	Prediction of the GaN HEMT performance based on the epitaxial material properties	87
5	GaN HEMTs on Native GaN Substrates	94
5.1	Comparative experiment design between GaN/GaN, GaN/Sapphire and GaN/Si	94
5.1.1	Choice of samples under investigation in the comparative study	95
5.1.2	Scope of characterization in the comparative study	97
5.2	Structural properties of GaN/GaN versus GaN on foreign substrates	97
5.2.1	GaN/GaN and GaN/Sapphire epitaxial layers description	97
5.2.2	TEM analyses of the GaN on different substrates	98
5.3	Electrical properties of GaN/GaN HEMTs	101
5.3.1	Static characteristics of GaN/GaN versus GaN/foreign substrates	101
5.3.2	Dynamic characteristics of GaN/GaN versus GaN/foreign substrates	106
5.3.3	Energy diffractive X-ray spectroscopy results for GaN/GaN and GaN/Sapphire epitaxial material	113

6 Thermal Characterization of GaN and Si chips	116
6.1 Indirect thermal investigations	117
6.1.1 Self-heating in GaN devices	117
6.1.2 Substrate temperature effect on GaN HEMTs	121
6.2 Direct thermal investigations	127
6.2.1 Thermal chip design	127
6.2.2 Transient thermal analysis	134
6.2.3 Steady-state surface temperature mapping	137
6.2.4 Thermal transfer function extraction methodology	142
7 Conclusion and outlook	151
A Scripts listing	154
A.1 Matlab scripts for statistical analyses	154
A.2 Skill scripts for layout generation	160
B Verilog-A HEMT Model	181
Bibliography	195
Author Publications	210
Curriculum Vitae	211